CLAIMS

1. An apparatus, for managing power consumption of a microprocessor comprising:

a plurality of functional units each including a corresponding plurality of activity outputs, for indicating when a respective functional unit is enabled;

utilization assessment logic, coupled to said plurality of activity outputs, for assessing activity thereof to determine a current total power consumption value for the microprocessor;

power control logic, coupled to said utilization assessment logic, for comparing said current total power consumption value with a threshold power value included in a specified power profile; and

a power consumption controller, coupled to said power management logic and said plurality of functional units, for engaging one of a plurality of power reduction modes if said current total power consumption value exceeds said threshold power value.

2. The apparatus as recited in claim 1, wherein one of said plurality of functional units is a cache and one of said plurality of power reduction modes is disabling said cache.

3. The apparatus as recited in claim 1, wherein one of said plurality of functional units is a branch prediction unit and one of said plurality of power reduction modes is disabling said branch prediction unit.

4. The apparatus as recited in claim 1, wherein one of said plurality of functional units is a floating point unit and one of said plurality of power reduction modes is disabling said floating point unit.

5. The apparatus as recited in claim 1, wherein one of said plurality of functional units is an MMX unit and one of said plurality of power reduction modes is disabling said MMX unit.

6. The apparatus as recited in claim 1, wherein one of said plurality of functional units is an execute unit and one of said plurality of power reduction modes is controlling power consumption of said execute unit by reducing a rate of issue of instructions to said execute unit.

7. The apparatus as recited in claim 1, further comprising a clock of predetermined frequency coupled to said plurality of functional units, wherein one of said plurality of power reduction modes comprises reducing the frequency of said clock.

8. The apparatus as recited in claim 1, further comprising a power supply voltage controller for controlling a supply voltage applied to said plurality of functional units, wherein one of said plurality of power reduction modes comprises reducing said supply voltage.

9. A microprocessor power management mechanism, comprising:

a plurality of functional units, each including an activity output for indicating when a respective functional unit is enabled;

power management logic, coupled to said activity outputs of the functional units, for assessing the activity of individual functional units to determine a current total power consumption value for a microprocessor; and

a power consumption controller, coupled to said power management logic and said plurality of functional units, for disabling or reducing the power consumption of at least one of said plurality of functional units, if said current total power consumption value exceeds a threshold power value.

10. The microprocessor power management mechanism as recited in claim 9, further comprising a control bus coupled between said power management logic and said power consumption controller.

11. The microprocessor power management mechanism as recited in claim 10, wherein said power control logic sends a command over said control bus to instruct said power consumption controller to disable a first one of said plurality of functional units if said current total power consumption value exceeds said threshold power value.

12. The microprocessor power management mechanism as recited in claim 10, wherein said power control logic sends a command over said control bus to instruct said power consumption controller to disable more than one of said plurality of functional units if said current total power consumption value exceeds said threshold power value.

13. The processor of claim 10 wherein said power management logic comprises:

utilization assessment logic, for processing activity output signals from said respective activity outputs to determine said current total power consumption value.

14. A method for managing power consumption in a microprocessor, the microprocessor including a plurality of functional units, the method comprising:

prescribing a power profile for the microprocessor, the power profile having a threshold power value;

assessing activity of the individual functional units to determine a current total power consumption value for the microprocessor;

comparing the current total power consumption value with the threshold power value; and

if the current total power consumption value exceeds the threshold power value, engaging one of a plurality of power reduction modes.

15. The method as recited in claim 14, wherein one of the plurality of power reduction modes includes disabling a first functional unit, the first functional unit being one of the plurality of functional units.

16. The method as recited in claim 15, wherein the first functional unit is a cache.

17. The method as recited in claim 15 wherein the first functional unit is a branch prediction unit.

18. The method as recited in claim 15, wherein the first functional unit is a floating point unit.

19. The method as recited in claim 15, wherein the first functional unit is an MMX unit.

20. The method as recited in claim 14, wherein said engaging comprises:

reducing a rate of issue of instructions to one or more of the plurality of functional units.

21. The method as recited in claim 14 wherein said engaging comprises:

reducing the frequency of a core clock within the microprocessor.

22. The method of claim 14, wherein said engaging comprises:

reducing an internal supply voltage from a first voltage to a second voltage.